IQS7222B DATASHEET

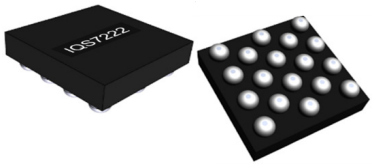
20 Channel Mutual / 8 Channel Self- Capacitive Touch and Proximity Controller with I²C communications interface, configurable GPIOs and low power options

1 Device Overview

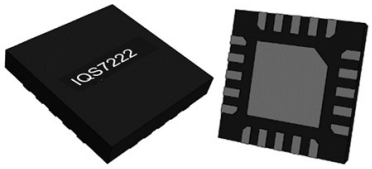
The IQS7222B ProxFusion® IC is a sensor fusion device for various multi-button applications. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) / 8 (WLCSP)external sensor pad connections
- Configure up to 20 Mutual capacitance buttons,18 mutual capacitance buttons with proximity wake-up function or up to 8 self-capacitance buttons[i]
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce & hysteresis
  - Dual direction trigger indication
- Design simplicity
  - PC Software for debugging and obtaining optimal settings and performance
  - One-time programmable settings for custom power-on IC configuration
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I2C communication interface with IRQ/RDY(up to fast plus -1MHz)
- Event and streaming modes
- Customizable user interface due to programmable memory
- Supply Voltage 1.8V(-5%)to 3.5V
- Small packages
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4mm x 0.6mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4mm pitch



WLCSP18 & QFN20 package
Representation only



1.2 Applications

- Remote Control User Interface
- Home Automation Device User Interface
- Wireless Speaker Controls

[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured is 18 buttons or 16 buttons with a wake-up function

1.3 Block Diagram

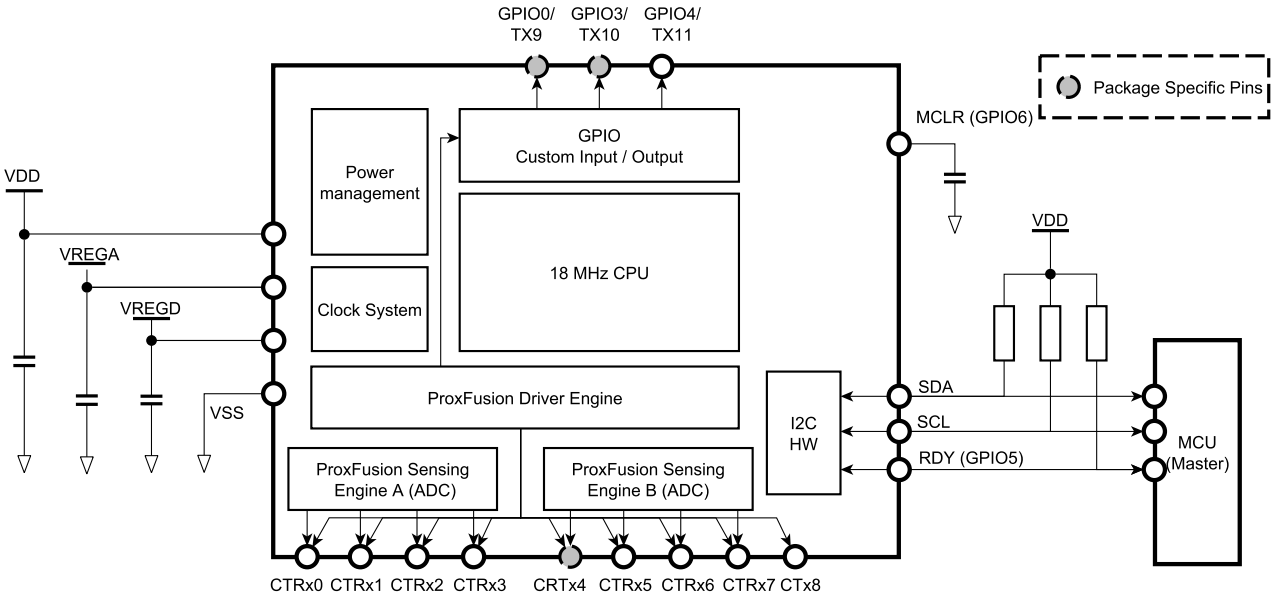


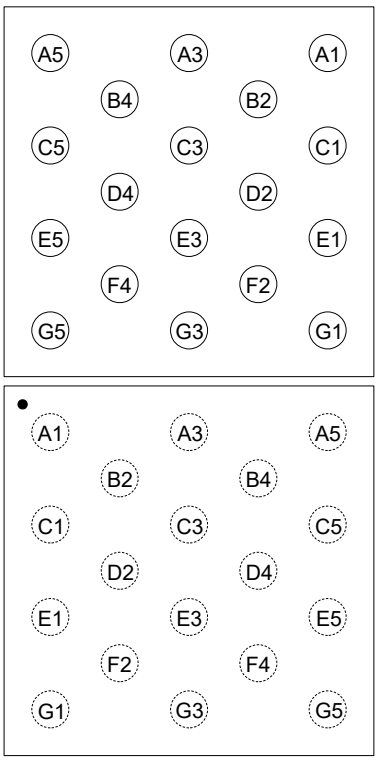
Figure 1.1: Functional Block Diagram[i]

[i] WLCSP18 packages do not have a CRx4 and combines GPIO and GPIO3

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

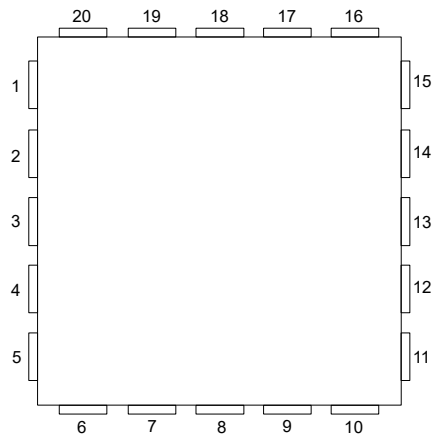
Table 2.1: 18-pin WLCSP18 Package (Bottom/Ball-side View)



Pin no.	Signal
A5	GPIO6 / MCLR
A3	SCL/ GPIO2
A1	Tx9/Tx10/GPIO0/GPIO3[i]
B4	SDA/GPIO1
B2	Tx11/GPIO4
C5	Vdd
C3	RDY/ GPIO5
C1	Tx8
D4	Vss
D2	CRx2/Tx2
E5	VregD
E3	CRx1/Tx1
E1	CRx6/Tx6
F4	CRx0/Tx0
F2	CRx5/Tx5
G5	VregA
G3	CRx3/Tx3
G1	CRx7/Tx7

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6
2	VREGD	12	CRx7
3	VSSD & VSSA	13	CTx8
4	VREGA	14	GPIO0
5	CRx0	15	GPIO3
6	CRx1	16	GPIO4
7	CRx2	17	GPIO5
8	CRx3	18	GPIO2
9	CRx4	19	GPIO1
10	CRx5	20	GPIO6

Area name	Signal name
Tab	Float

[i]Please note that Tx9 and Tx10 are shorted in the WLCSP18 package

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no. WLCSP18	Pin no. QFN20	Signal name	Signal type[ii]	Buffer type	Power source	Reset state after BOR[iii]
C5	1	VDD	Power	Power	N/A	
E5	2	VREGD	Power	Power	N/A	
D4	3	VSSA & VSSD	Power	Power	N/A	
G5	4	VREGA	Power	Power	N/A	
F4	5	CRx0/Tx0	Analog		VREGA	
E3	6	CRx1/Tx1	Analog		VREGA	
D2	7	CRx2/Tx2	Analog		VREGA	
G3	8	CRx3/Tx3	Analog		VREGA	
-	9	CRx4/Tx4	Analog		VREGA	
F2	10	CRx5/Tx5	Analog		VREGA	
E1	11	CRx6/Tx6	Analog		VREGA	
G1	12	CRx7/Tx7	Analog		VREGA	
C1	13	CTx8	Analog		VREGA	
A1	14	GPIO0/Tx9	Digital/Prox		VDD/VREGA	
B4	19	SDA/GPIO1	Digital		VDD	
A3	18	SCL/GPIO2	Digital		VDD	
A1	15	GPIO3/Tx10	Digital/Prox		VDD/VREGA	
B2	16	GPIO4/Tx11	Digital/Prox		VDD/VREGA	
C3	17	RDY/GPIO5	Digital/Prox		VDD	
A5	20	MCLR/GPIO6	Digital		VDD	

[ii] Signal Types: I = Input, O = Output, I/O = Input or Output
[iii] High-Z = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no. WLCSP18	Pin no. QFN20	Pin type	Description
ProxFusion®	CRx0	F4	5	IO	ProxFusion® channel
	CRx1	E3	6	IO	
	CRx2	D2	7	IO	
	CRx3	G3	8	IO	
	CRx4	-	9	IO	
	CRx5	F2	10	IO	
	CRx6	E1	11	IO	
	CRx7	G1	12	IO	
	CTx8	C1	13	IO	
	CTx9/ GPIO0	A1	14	IO	CTx9 pad
	CTx10/GPIO3	A1	15	IO	CTx10 pad
	CTx11GPIO4	B2	16	IO	CTx11 pad
	CTx12/GPIO5	C3	17	IO	Input filter disabled for external clock input.
GPIO	MCLR/ GPIO6	A5	20	IO	Active pulldown, 200k resistor to VDD, Pulled low during POR, and MCLR function enabled by default. VPP input for OTP
I2C	SDA/GPIO1	B4	19	IO	I2C Data
	SCL/GPIO2	A3	20	IO	I2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSSA/VSSD	D4	3	P	Analog/Digital Ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

2.5 Reference Schematic

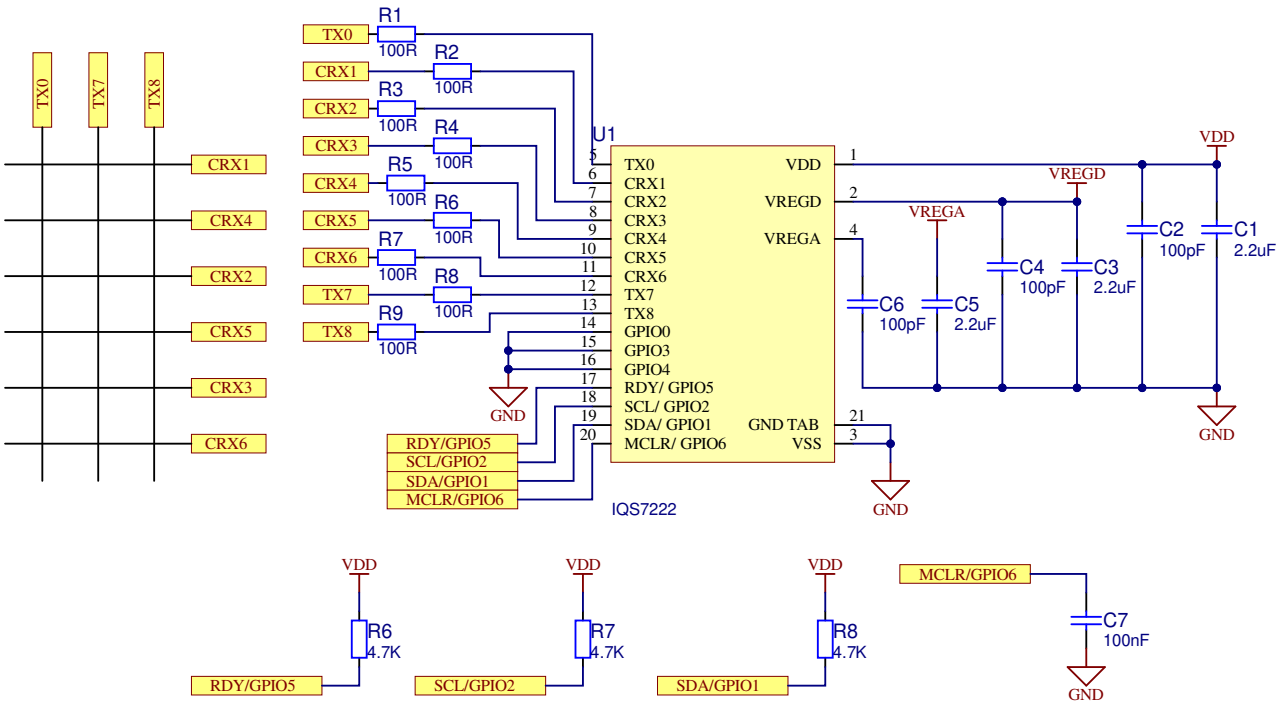


Figure 2.1: 18 Button Mutual Capacitance Reference Schematic

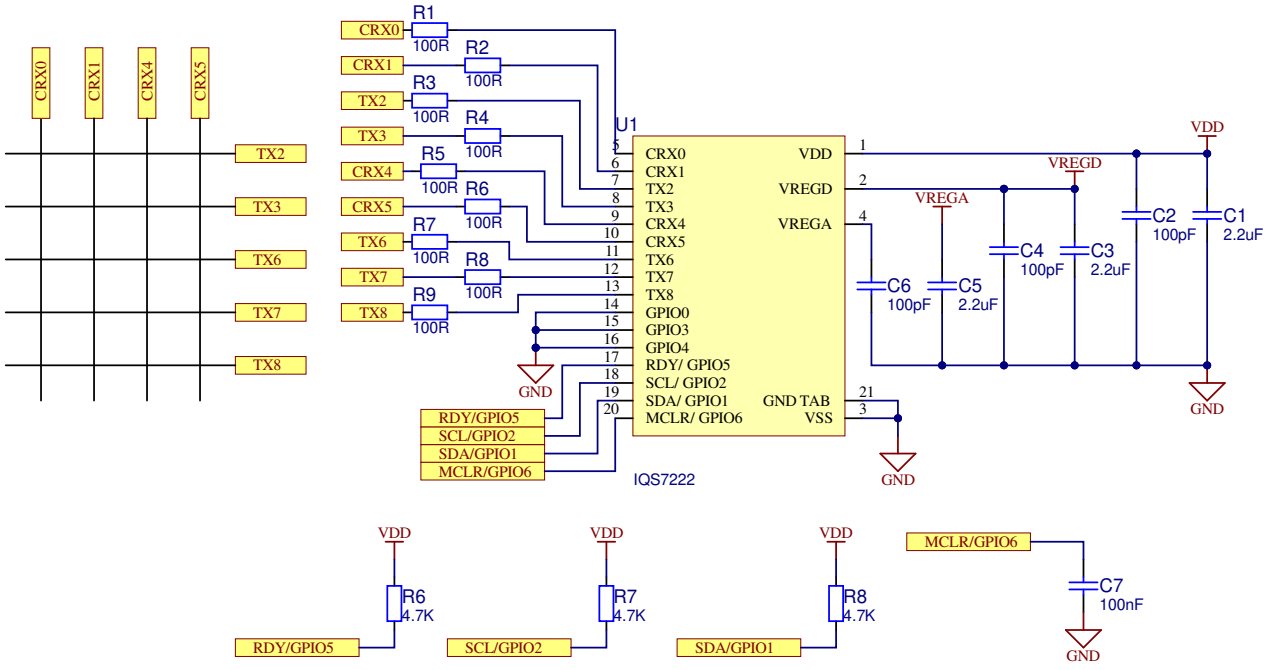


Figure 2.2: 20 Button Mutual Capacitance Reference Schematic

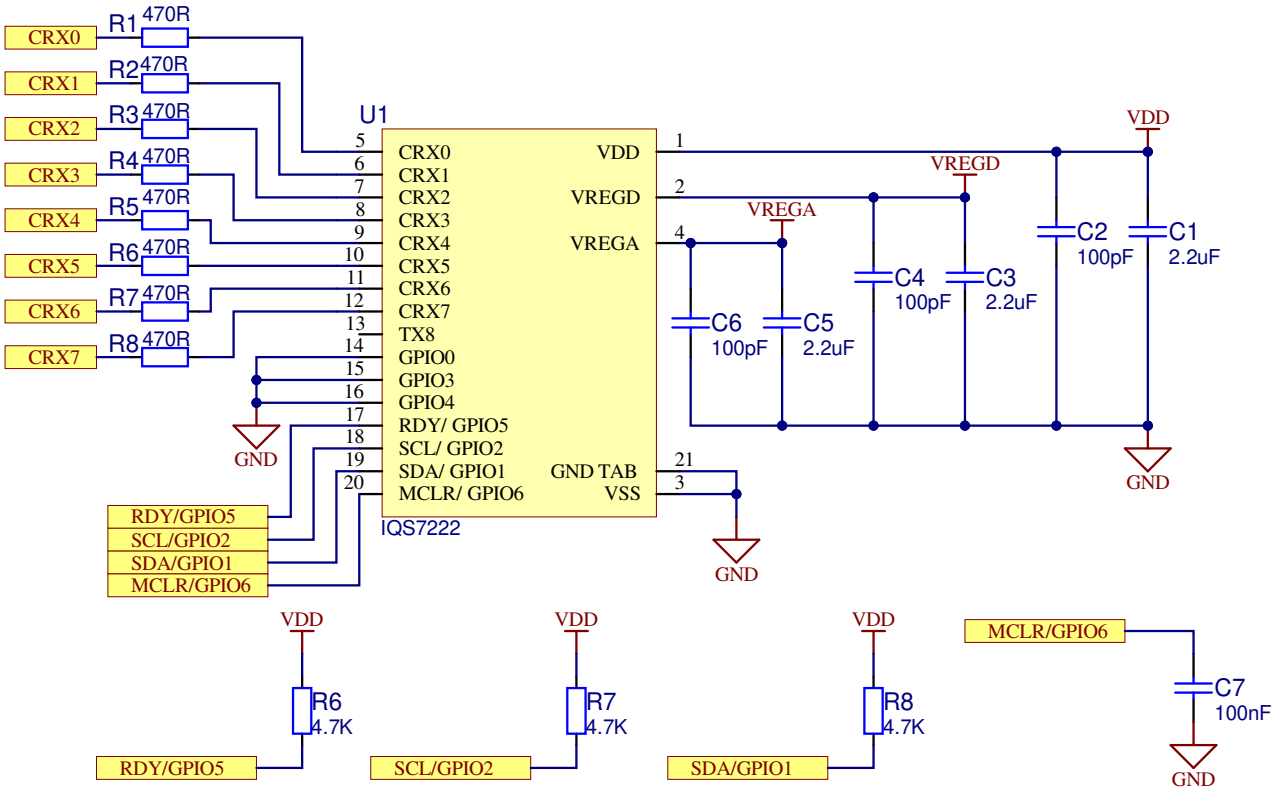


Figure 2.3: 8 Button Self Capacitance Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.5V max)	V
Storage temperature, T_{stg}	-40	85	℃

3.2 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[i]	± 4000	V

3.3 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.5	V
VregA	Internal regulated supply output for analog domain	1.5	1.53	1.75	V
VregD	Internal regulated supply output for digital domain	1.57	1.59	1.8[ii]	V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	-40	25	85	℃
C_{VDD}	Recommended capacitor at VDD	1	2	10	µF
C_{VREGA}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	1	2	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	1	2	10	µF
$Cx_{\_SELF-VSS}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (self-capacitance mode)	-	-	400	pF
$Cm_{\_CTX-CRX}$	Capacitance of all external electrodes on all ProxFusion® blocks (mutual-cap mode)	0.1	-	90	pF
$Cx_{\_CRX-VSS-1M}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @f_{xfer}=1MHz)			100	pF
$Cx_{\_CRX-VSS-4M}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f_{xfer}=4MHz sensing))			25	pF
$\frac{Cx_{CRX-VSS}}{Cm_{CTX-CRX}}$	Capacitance ratio for optimal SNR in mutual capacitance mode	10		20	n/a
$RCx_{\_CRX/CTX}$	Series (in-line) resistance of all mutual capacitance pins (Tx & Rx pins) in mutual capacitance mode	0[iii]	0.47	10[iv]	kΩ
$RCx_{\_SELF}$	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0[ii]	0.47	10[iv]	kΩ

[i] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

[ii] Vdd≥2V

[iii] Nominal series resistance of 470Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection

[iv] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. R_{max} x C_{max} = $\frac{1}{(6x f_{xfer})}$ where "C" is the pin capacitance to Vss.

3.4 Current Consumption

Projected Mode Setup: Target: CH0 & CH10 = 800, all other channels = 512
Self-capacitive Mode Setup: Target = 512, Fxfer = 500kHz
Interface Selection: Event mode

Power mode	Active channels	Report rate (Sampling rate) [ms]	Current [µA]
Active Mode	Mutual Capacitance (20 channels)	10	1420
	Self-capacitive (8 channels)	10	610
Idle	Mutual Capacitance (20 channels)	50	260
	Self-capacitive (8 channels)	50	120
ULP	Wake-up proximity - Distributed mutual channel	100	15
	Wake-up proximity - Distributed self channel	100	13
ULP	Wake-up proximity - Distributed mutual channel	160	10
	Wake-up proximity - Distributed self channel	160	9

4 Timing and Switching Characteristics

4.1 Reset Levels

		Min	Typ	Max	Unit
V_{VDDHI}	Power-up/down level (Reset trigger) - slope >100V/s	1.040	1.353	1.568	V
V_{REG}	Power-up/down level (Reset trigger) - slope >100V/s	0.945	1.122	1.304	V

4.2 MCLR Pin Levels and Characteristics

Table 4.1: MCLR Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(MCLR)VDD\_HI}$	MCLR Input high level voltage	Vdd = 3.3V	VSS-0.3	-	1.05	V
$V_{IL(MCLR)VDD\_LOW}$	MCLR Input low level voltage	Vdd = 1.7V	VSS-0.3	-	0.75	V
$V_{IH(MCLR)VDD\_HI}$	MCLR Input high level voltage	Vdd = 3.3V	2.25	-	VDD_HI+0.3	V
$V_{IH(MCLR)VDD\_HI}$	MCLR Input high level voltage	Vdd = 1.7V	1.05	-	VDD_LOW+0.3	V
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width - no trigger	Vdd = 3.3V	-	-	15	ns
$t_{PULSE(MCLR)}$	MCLR input pulse width - no trigger	Vdd = 1.7V			10	ns
$t_{TRIG(MCLR)}$	MCLR input pulse width - ensure trigger	Vdd = 3.3V, Vdd = 1.7V	250	-	-	ns

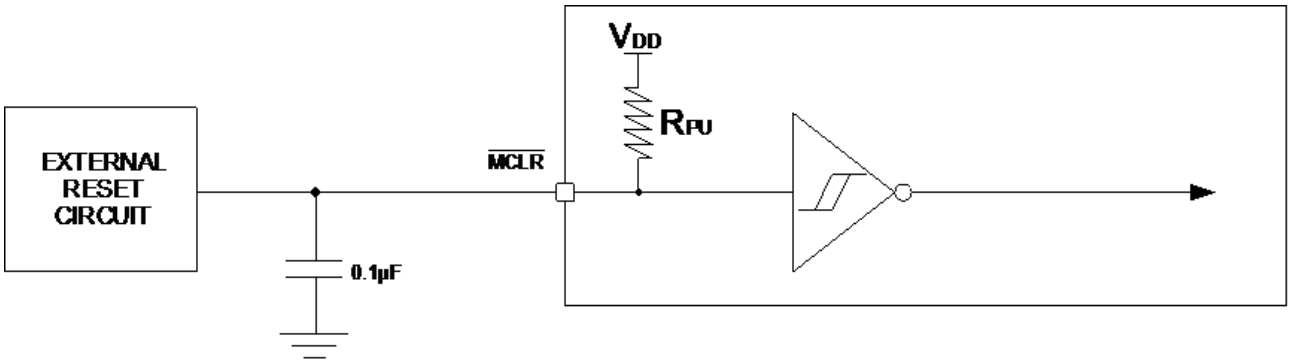


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{SYS})	42	500-1500	5000	kHz
f_{OSC}	Master CLK frequency tolerance 14MHz	13.23	14	14.77	MHz
f_{OSC}	Master CLK frequency tolerance 18MHz	17.1	18	19.54	MHz
t_{WDT}	Software watchdog timer period		1024		ms

4.4 Digital I/O Characteristics

		min	nom	max	Unit
V_{IL}	Input low level voltage	Vss -0.3V		0.3 * VDDHI	V
V_{IH}	Input high level voltage	0.7 * VDDHI		VDDHI + 0.3V	V

4.5 I²C Characteristics

PARAMETER		TEST CONDITIONS	VDDHI	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		1.8V, 3.3V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		1.8V, 3.3V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START		1.8V, 3.3V	0.26			µs
$t_{HD,DAT}$	Data hold time		1.8V, 3.3V	0			ns
$t_{SU,DAT}$	Data setup time		1.8V, 3.3V	50			ns
$t_{SU,STO}$	Setup time for STOP		1.8V, 3.3V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		1.8V, 3.3V	50			ns

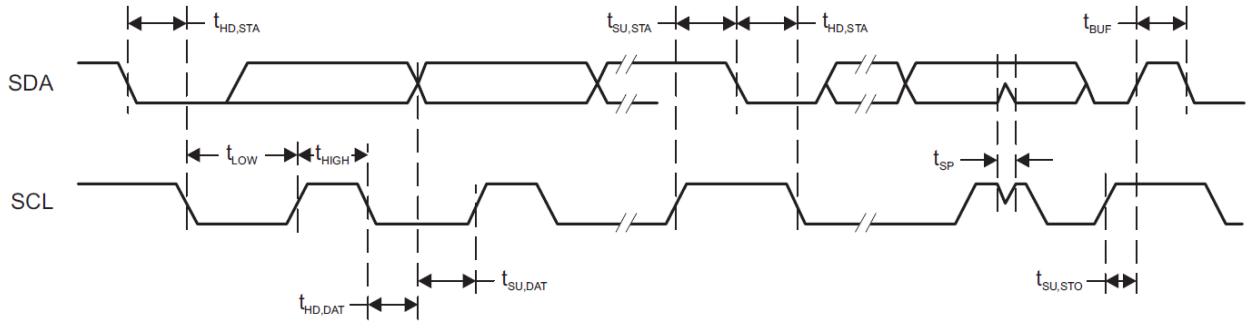


Figure 4.2: I²C Mode Timing Diagram

5 ProxFusion® Module

The IQS7222B contains dual ProxFusion® modules that uses patented technology to measure and process the capacitive sensor data. Two modules ensure a rapid response from multi-button implementations. The multiple touch & proximity outputs are the primary output from the sensor.

5.1 Capacitive Channels

Mutual capacitance and Self capacitance designs are possible with the IQS7222B.

- Sensor pad design overview: AZD008
- Mutual capacitance (also known as Projected capacitance) button layout guide: AZD036

5.2 Low Power Options

The IQS7222B offers 3 power modes:

- Normal power mode (NP)
  - Flexible key scan rate
- Lower power mode (LP)
  - Flexible key scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are typically sampled at a slower rate in order to optimize power consumption

5.3 Count Value

The capacitive sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance, and all outputs are derived from this.

5.3.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit *(Maximum counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.4 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.4.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0xD0, bit3).

5.5 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please see contact Azoteq.

5.6 Automatic Re-ATI

5.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7222B, a status bit will set momentarily to indicate that this has occurred.

5.6.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.12.

$$\textbf{Re-ATI Boundary}_{\textbf{default}} = \textbf{ATI target} \pm (\tfrac{1}{16}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and that the and the default boundary value is 1/16*800 = 50. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

Reference > 850 or Reference < 750

The ATI algorithm executes in a short time, so goes unnoticed by the user.

5.6.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

6 Sensing Modes

6.1 Mode Timeout

In order to optimize power consumption and performance, power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time know as the "mode timeout".

6.2 Count Filter

6.2.1 IIR Filter

The IIR filter applied to the digitized raw input offers various damping options as defined in Table A.18 and Table A.19

Damping factor = Beta/256

7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Below some are described, the other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*, if it becomes set again, the master will know a reset has occurred, and can react appropriately.

7.2.2 Software Reset

The IQS7222B can be reset by means of an I^2C command (*Soft Reset*).

8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific firmware is exported by the GUI and programmed onto the device. These parameters are used as the default values after start-up, without requiring any setup from the master.

8.2 Automated Start-up

The device is programmed with the application firmware, bundled with settings specifically configured for the current hardware as described in Section 8.1. After power-up the device will automatically use the settings and perform the configuration/setup accordingly.

8.3 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.

8.4 RF Immunity

The IQS7222B has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DDHI}.

Place a 100pF in parallel with the 2.2μF ceramic on V_{REG}. Place a 2.2μF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470Ω-1kΩ. PCB ground planes also improve noise immunity.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7222B supports the following:

- *Fast-mode-plus* standard I2C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7222B implements 8-bit addressing with 2 bytes at each address with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The default 7-bit device address is 0x56 ('1010110'). The full address byte will thus be 0xAD (read) or 0xAC (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement 16-bit addressing scheme.

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive, however the corresponding data was missed/lost, and this should be avoided.

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected.

9.9 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9.1 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.2, Table A.3 and Table A.2:

- Power mode change
- Prox or touch event
- ATI error
- ATI active
- ATI Event
- Power mode change

9.9.2 Force Communication / Polling

The master can initiate communication even while RDY is HIGH (inactive). The IQS7222B will clock stretch until an appropriate time to complete the I^2C transaction. The master firmware will not be affected (if clock stretching is correctly handled).

For optimal program flow, it is suggested that RDY is used to sync on new data. The forced/polling method is only recommended if the master must perform I^2C and *Event Mode* is active

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
0x10	System Status	See Table A.2
0x11	Events	See Table A.3
0x12	Prox event States	See Table A.4
0x13		See Table A.5
0x14	Touch event States	See Table A.6
0x15		See Table A.7
	Channel Counts	
0x20	Channel 0 Counts	16-bit value
0x21	Channel 1 Counts	
0x22	Channel 2 Counts	
0x23	Channel 3 Counts	
0x24	Channel 4 Counts	
0x25	Channel 5 Counts	
0x26	Channel 6 Counts	
0x27	Channel 7 Counts	
0x28	Channel 8 Counts	
0x29	Channel 9 Counts	
0x2A	Channel 10 Counts	
0x2B	Channel 11 Counts	
0x2C	Channel 12 Counts	
0x2D	Channel 13 Counts	
0x2E	Channel 14 Counts	
0x2F	Channel 15 Counts	
0x30	Channel 16 Counts	
0x31	Channel 17 Counts	
0x32	Channel 18 Counts	
0x33	Channel 19 Counts	
	Channel LTA	
0x40	Channel 0 LTA	16-bit value
0x41	Channel 1 LTA	
0x42	Channel 2 LTA	
0x43	Channel 3 LTA	
0x44	Channel 4 LTA	
0x45	Channel 5 LTA	
0x46	Channel 6 LTA	
0x47	Channel 7 LTA	
0x48	Channel 8 LTA	
0x49	Channel 9 LTA	
0x4A	Channel 10 LTA	
0x4B	Channel 11 LTA	
0x4C	Channel 12 LTA	
0x4D	Channel 13 LTA	
0x4E	Channel 14 LTA	
0x24	Channel 15 LTA	
0x50	Channel 16 LTA	
0x51	Channel 17 LTA	
0x52	Channel 18 LTA	
0x53	Channel 19 LTA	
	Cycle Setup	
0x8000	Cycle Setup 0	See Table A.8
0x8001		See Table A.9
0x8100	Cycle Setup 1	See Table A.8
0x8101		See Table A.9
0x8200	Cycle Setup 2	See Table A.8
0x8201		See Table A.9

0x8300	Cycle Setup 3	See Table A.8
0x8301		See Table A.9
0x8400	Cycle Setup 4	See Table A.8
0x8401		See Table A.9
0x8500	Cycle Setup 5	See Table A.8
0x8501		See Table A.9
0x8600	Cycle Setup 6	See Table A.8
0x8601		See Table A.9
0x8700	Cycle Setup 7	See Table A.8
0x8701		See Table A.9
0x8800	Cycle Setup 8	See Table A.8
0x8801		See Table A.9
0x8900	Cycle Setup 9	See Table A.8
0x8901		See Table A.9
0x8A00	Global Cycle Setup	See Table A.10
	Channel Setup	
0x9000	Channel Setup 0	See Table A.11
0x9001		See Table A.12
0x9100	Channel Setup 1	See Table A.11
0x9101		See Table A.12
0x9200	Channel Setup 2	See Table A.11
0x9201		See Table A.12
0x9300	Channel Setup 3	See Table A.11
0x9301		See Table A.12
0x9400	Channel Setup 4	See Table A.11
0x9401		See Table A.12
0x9500	Channel Setup 5	See Table A.11
0x9501		See Table A.12
0x9600	Channel Setup 6	See Table A.11
0x9601		See Table A.12
0x9700	Channel Setup 7	See Table A.11
0x9701		See Table A.12
0x9800	Channel Setup 8	See Table A.11
0x9801		See Table A.12
0x9900	Channel Setup 9	See Table A.11
0x9901		See Table A.12
0x9A00	Channel Setup 10	See Table A.11
0x9A01		See Table A.12
0x9B00	Channel Setup 11	See Table A.11
0x9B01		See Table A.12
0x9C00	Channel Setup 12	See Table A.11
0x9C01		See Table A.12
0x9D00	Channel Setup 13	See Table A.11
0x9D01		See Table A.12
0x9E00	Channel Setup 14	See Table A.11
0x9E01		See Table A.12
0x9F00	Channel Setup 15	See Table A.11
0x9F01		See Table A.12
0xA000	Channel Setup 16	See Table A.11
0xA001		See Table A.12
0xA100	Channel Setup 17	See Table A.11
0xA101		See Table A.12
0xA200	Channel Setup 18	See Table A.11
0xA201		See Table A.12
0xA300	Channel Setup 19	See Table A.11
0xA301		See Table A.12
	Channel Setup Channel 0	
0xB000	CRX Select and General Channel Setup	See Table A.13
0xB001	ATI Base and Target	See Table A.15
0xB002	Fine and Coarse Multipliers	See Table A.16

0xB003	ATI Compensation	See Table A.17
	Channel 1	
0xB100	CRX Select and General Channel Setup	See Table A.13
0xB101	ATI Base and Target	See Table A.15
0xB102	Fine and Coarse Multipliers	See Table A.16
0xB103	ATI Compensation	See Table A.17
	Channel 2	
0xB200	CRX Select and General Channel Setup	See Table A.13
0xB201	ATI Base and Target	See Table A.15
0xB202	Fine and Coarse Multipliers	See Table A.16
0xB203	ATI Compensation	See Table A.17
	Channel 3	
0xB300	CRX Select and General Channel Setup	See Table A.13
0xB301	ATI Base and Target	See Table A.15
0xB302	Fine and Coarse Multipliers	See Table A.16
0xB303	ATI Compensation	See Table A.17
	Channel 4	
0xB400	CRX Select and General Channel Setup	See Table A.13
0xB401	ATI Base and Target	See Table A.15
0xB402	Fine and Coarse Multipliers	See Table A.16
0xB403	ATI Compensation	See Table A.17
	Channel 5	
0xB500	CRX Select and General Channel Setup	See Table A.13
0xB501	ATI Base and Target	See Table A.15
0xB502	Fine and Coarse Multipliers	See Table A.16
0xB503	ATI Compensation	See Table A.17
	Channel 6	
0xB600	CRX Select and General Channel Setup	See Table A.13
0xB601	ATI Base and Target	See Table A.15
0xB602	Fine and Coarse Multipliers	See Table A.16
0xB603	ATI Compensation	See Table A.17
	Channel 7	
0xB700	CRX Select and General Channel Setup	See Table A.13
0xB701	ATI Base and Target	See Table A.15
0xB703	Fine and Coarse Multipliers	See Table A.16
0xB704	ATI Compensation	See Table A.17
	Channel 8	
0xB800	CRX Select and General Channel Setup	See Table A.13
0xB801	ATI Base and Target	See Table A.15
0xB802	Fine and Coarse Multipliers	See Table A.16
0xB803	ATI Compensation	See Table A.17
	Channel 9	
0xB900	CRX Select and General Channel Setup	See Table A.13
0xB901	ATI Base and Target	See Table A.15
0xB902	Fine and Coarse Multipliers	See Table A.16
0xB903	ATI Compensation	See Table A.17
	Channel 10	
0xBA00	CRX Select and General Channel Setup	See Table A.14
0xBA01	ATI Base and Target	See Table A.15
0xBA02	Fine and Coarse Multipliers	See Table A.16
0xBA03	ATI Compensation	See Table A.17
	Channel 11	
0xBB00	CRX Select and General Channel Setup	See Table A.14
0xBB01	ATI Base and Target	See Table A.15
0xBB02	Fine and Coarse Multipliers	See Table A.16
0xBB03	ATI Compensation	See Table A.17
	Channel 12	
0xBC00	CRX Select and General Channel Setup	See Table A.14
0xBC01	ATI Base and Target	See Table A.15
0xBC02	Fine and Coarse Multipliers	See Table A.16

0xBC03	ATI Compensation		See Table A.17
	Channel 13		
0xBD00	CRX Select and General Channel Setup		See Table A.14
0xBD01	ATI Base and Target		See Table A.15
0xBD02	Fine and Coarse Multipliers		See Table A.16
0xBD03	ATI Compensation		See Table A.17
	Channel 14		
0xBE00	CRX Select and General Channel Setup		See Table A.14
0xBE01	ATI Base and Target		See Table A.15
0xBE02	Fine and Coarse Multipliers		See Table A.16
0xBE03	ATI Compensation		See Table A.17
	Channel 15		
0xBF00	CRX Select and General Channel Setup		See Table A.14
0xBF01	ATI Base and Target		See Table A.15
0xBF02	Fine and Coarse Multipliers		See Table A.16
0xBF03	ATI Compensation		See Table A.17
	Channel 16		
0xC000	CRX Select and General Channel Setup		See Table A.14
0xC001	ATI Base and Target		See Table A.15
0xC002	Fine and Coarse Multipliers		See Table A.16
0xC003	ATI Compensation		See Table A.17
	Channel 17		
0xC100	CRX Select and General Channel Setup		See Table A.14
0xC101	ATI Base and Target		See Table A.15
0xC103	Fine and Coarse Multipliers		See Table A.16
0xC103	ATI Compensation		See Table A.17
	Channel 18		
0xC200	CRX Select and General Channel Setup		See Table A.14
0xC201	ATI Base and Target		See Table A.15
0xC203	Fine and Coarse Multipliers		See Table A.16
0xC203	ATI Compensation		See Table A.17
	Channel 19		
0xC300	CRX Select and General Channel Setup		See Table A.14
0xC301	ATI Base and Target		See Table A.15
0xC303	Fine and Coarse Multipliers		See Table A.16
0xC303	ATI Compensation		See Table A.17
	Filter Betas		
0xC400	Filter Beta		See Table A.18
0xC401	Fast Filter Beta		See Table A.19
	PMU and System Settings		
0xD0	Control settings		See Table A.20
0xD1	ATIErrorATI Error Timeout		16-bit value (ms)
0xD2	ATI Report Rate		16-bit value (ms)
0xD3	Normal Power Mode Timeout		16-bit value (ms)
0xD4	Normal Power Mode Report Rate		16-bit value (ms)
0xD5	Low Power Mode Timeout		16-bit value (ms)
0xD6	Low Power Mode Report Rate		16-bit value (ms)
0xD7	Normal Power Update rate in Ultra-low Power Mode		16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate		16-bit value (ms)
0xD9	Touch Event Timeout	Prox Event Timeout	8-bit value in 500ms steps

11 Applications, Implementation and Layout

11.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 2.2-µF plus a 100-pF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

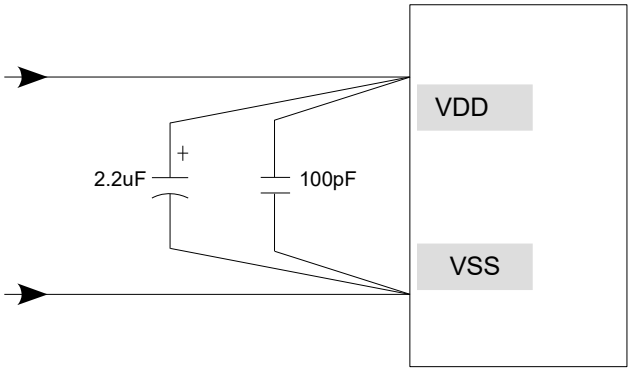


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 Transient Signal Management

During power up, power down, and device operation, VDD must not exceed the absolute maximum ratings. Exceeding the specified limits may cause malfunction of the device.

11.1.3 ProxFusion® Peripheral

This section provides a brief introduction to the ProxFusion® technology with examples of PCB layout and performance from a design kit. Please contact Azoteq for more details on design variables not covered here.

11.1.4 VREG

The VREG pin requires a 2.2-µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the microcontroller. The figure below shows an example layout where the capacitor is placed close to the IC.

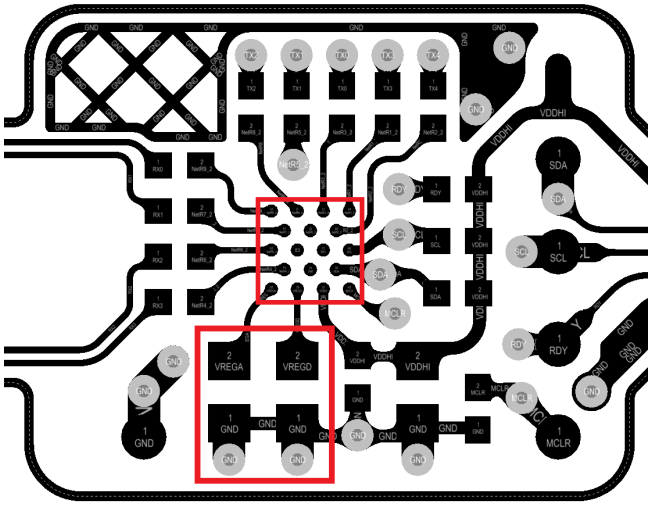


Figure 11.2: VREG Capacitor Placement Close to IC

11.1.5 ESD Protection

Typically, the laminate overlay provides several kilovolts of breakdown isolation to protect the circuit from ESD strikes. More ESD protection can be added with a series resistor placed on each channel used. A value of 470 Ω is recommended.

11.1.6 Self-capacitance Electrode Design

Self-capacitance electrodes are characterized by having only one channel from the IC that both excites and measures the capacitance. The capacitance being measured is between the electrode and circuit ground, so any capacitance local to the PCB or outside of the PCB (a touch event) influences the measurement.

For PCB layout design it is important to minimize local parasitic capacitances while shielding (with circuit GND) the self-capacitance traces against mechanical changes, induced noise and temperature effects of the board material. Minimize the local parasitic capacitances in order to maximize the effect of external capacitances (proximity and touch effects). To minimize parasitic effects on the PCB, the ground pour on the bottom layer is hatched and there is no pour directly below the electrode: 1.27mm spacing between the electrode and ground fill.

11.1.7 ATI (Auto Tuning Implementation)

The ATI process adjusts three values (Coarse multiplier, Fine multiplier, Compensation) using two parameters per plate (ATI base and ATI target). The ATI process is used to ensure that the sensor's sensitivity is not severely affected by external influences (Temperature, voltage supply change, etc.). For a detailed description of ATI, please contact Azoteq.

12 Ordering Information

IQS7222B zzz ppb

IC NAME	IQS7222B	=	IQS7222B	
POWER-ON CONFIGURATION	zzz	=	001	18 Button settings (mutual capacitance) with proximity wake-up
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QN	QFN-20 package
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Figure 12.1: Order Code Description

13 Package Specification

13.1 Package Outline Description - WLCSP18

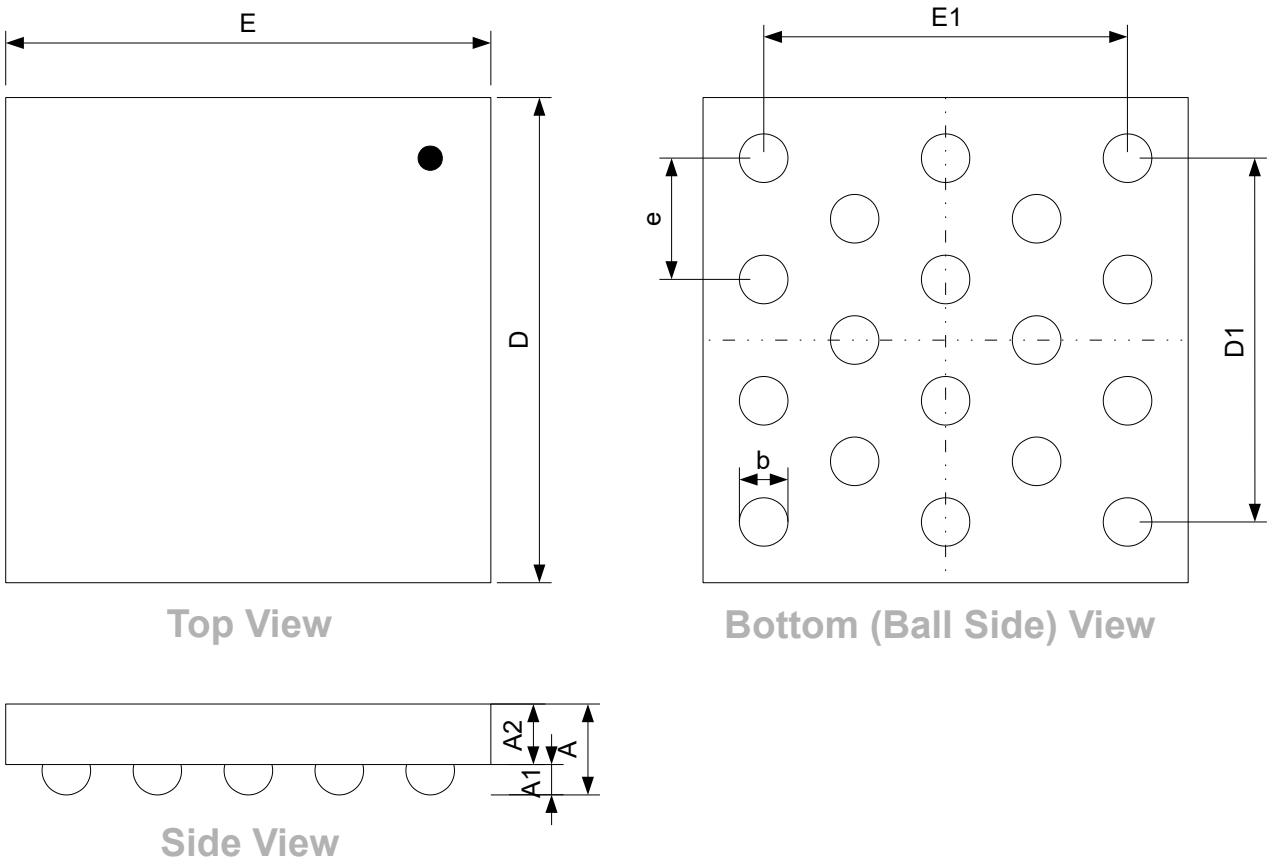


Figure 13.1: WLCSP (1.62x1.62) - 18 Package Outline Visual Description

Table 13.1: WLCSP (1.62x1.62) - 18 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.525±0.05	D1	1.2
A1	0.2±0.02	E	1.620±0.015
A2	0.3±0.025	E1	1.2
b	0.260±0.39	e	0.4
D	1.620±0.015		

13.2 Package Outline Description - QFN20

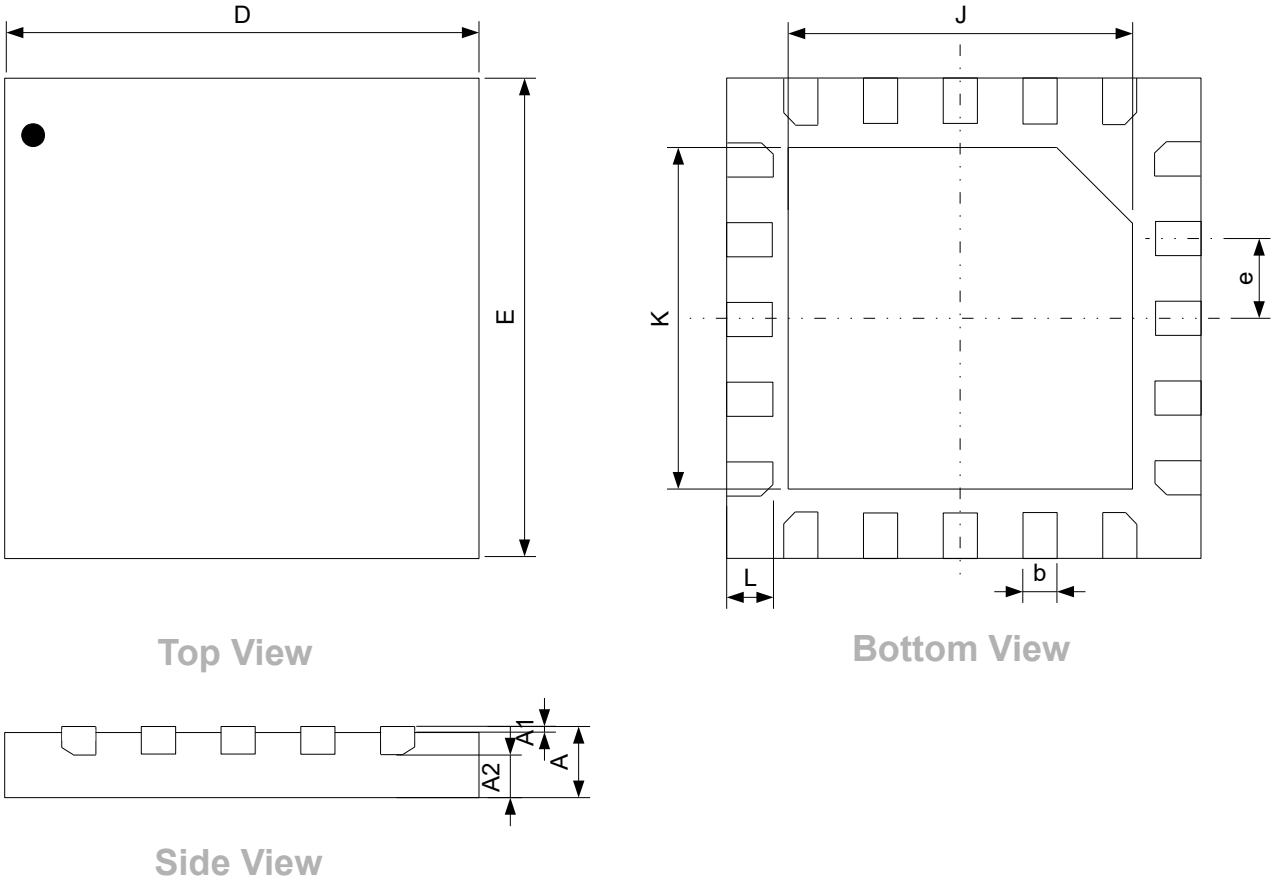


Figure 13.2: QFN (3x3)-20 Package Outline Visual Description

Table 13.2: QFN (3x3)-20 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.5±0.1	E	3
A1	0.035±0.05	e	0.4
A2	0.3	J	1.7±0.1
A3	0.203	K	1.7±0.1
b	0.2±0.05	L	0.4±0.05
D	3		

13.3 Moisture Sensitivity Levels

Contact Azoteq

13.4 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Table A.1: Version Information

Register:	0x00 - 0x09		
Address	**Category**	**Name**	**Value**
0x00	Application Version Info	Product Number	698
0x01		Major Version	1
0x02		Minor Version	20
0x03		Patch Number (Commit hash)	Value between 0 and 65536
0x04			
0x05	ROM Library Version Info	Library Number	595
0x06		Major Version	0
0x07		Minor Version	33
0x08		Patch Number (Commit hash)	TBC
0x09			

Table A.2: System Status

Register:	0x10														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	NP update	Power mode		Reset	Res	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active
- Bit 6: **NP Update**
  - 0: No Normal Power Update occured
  - 1: Normal Power update occured
- Bit 4-5: **Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.3: Events

Register:	0x11														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Reserved										Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.4: Proximity Event States 0

Register:	0x12														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-15: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

Table A.5: Proximity Event States 1

Register:		0x13													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												CH19	CH18	CH17	CH16

- Bit 0-3: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

Table A.6: Touch Event States 0

Register:		0x14													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-15: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.7: Touch Event States 1

Register:		0x15													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												CH19	CH18	CH17	CH16

- Bit 0-3: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.8: Cycle Setup 0

Register:		0x800, 0x8100, 0x8200, 0x8300, 0x8400, 0x8500, 0x8600, 0x8700, 0x8800, 0x8900													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 8-15: **Conversion Period**
  - $\frac{128}{FrequencyFraction} - 2$
  - Range: 0 - 127
- Bit 0-7: **Frequency Fraction**
  - $256 * \frac{f_{conv}}{f_{clk}}$
  - Range: 0 - 255

Table A.9: Cycle Setup 1

Register:		0x801, 0x8101, 0x8201, 0x8301, 0x8401, 0x8501, 0x8601, 0x8701, 0x8801, 0x8901													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	Inactive Rx - GND	Dead time en- abled	FOSC TX Freq	Vbias en- able	PXS Mode		

- Bit 15: **Tx8**
  - 0: Tx8 disabled
  - 1: Tx8 enabled
- Bit 14: **Tx7**
  - 0: Tx7 disabled
  - 1: Tx7 enabled
- Bit 13: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 12: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled

- Bit 11: **Tx4**
  - 0: Tx4 disabled
  - 1: Tx4 enabled
- Bit 10: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 9: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 8: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 7: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled
- Bit 6: **Inactive Rx GND**
  - 0: Inactive Rx floating
  - 1: Inactive Rx Grounded
- Bit 5: **Dead Time Enabled**
  - 0: Deadtime disabled
  - 1: Deadtime enabled
- Bit 4: **TX FOSC Frequency**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Vbias Enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-2: **PXS Mode**
  - 000: None
  - 001: Self-capacitive
  - 010: Projected capacitance
  - 011: Mutual inductance

Table A.10: Global Cycle Setup

Register:	0x8A00														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RF Filter EN	Maximum counts		Reserved					1	1	00		Auto Mode		Reserved	

- Bit 15: **RF Filter Enable**
  - 0: RF Filter disabled
  - 1: RF Filter enabled
- Bit 13-14: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 2-3: **Auto Mode**
  - Number of conversions created before each interrupt is generated
  - 00: 4
  - 01: 8
  - 10: 16
  - 11: 32

Table A.11: Channel Setup 0

Register:	0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700, 0x9800, 0x9900, 0x9A00, 0x9B00, 0x9C00, 0x9D00, 0x9E00, 0x9F00, 0xA000 0xA100, 0xA200, 0xA300														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value

- Bit 8-11: **Enter Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 0-7: **Proximity Threshold**
  - 8-bit value

Table A.12: Channel Setup 1

Register: 0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701, 0x9801, 0x9901, 0x9A01, 0x9B01, 0x9C01, 0x9D01, 0x9E01, 0x9F01, 0xA001, 0xA101, 0xA201, 0xA301

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{LTA}{2^{16}}$*(Threshold bit value - Hysteresis bit value)
- Bit 0-7: **Touch Threshold**
  - $\frac{LTA}{256} * 16\text{bit value}$

Table A.13: CRX Select and General Channel Setup(CH0-Ch9)

Register: 0xB000, 0xB100, 0xB200, 0xB300, 0xB400, 0xB500, 0xB600, 0xB700, 0xB800, 0xB900

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		ATI Band		Global halt	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs 80pF	0v5 Rev	Proj Bias Select	

- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled
- Bit 6: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled
- Bit 5: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled
- Bit 4: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled
- Bit 3: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vbias enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA

- 11: 10μA

Table A.14: CRX Select and General Channel Setup(CH10-Ch19)

Register:	0xBA00, 0xBB00, 0xBC00, 0xBD00, 0xBE00, 0xBF00, 0xC000, 0xC100, 0xC200, 0xC300														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		ATI Band		Global halt	Invert	Dual	Enabled	CRX4	CRX5	CRX6	CRX7	Cs 80pF	0v5 Rev	Proj Bias Select	

> Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
> Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with golbal halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
  - 0: Halt disabled
  - 1: Halt enabled
> Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
> Bit 9: **Bi-directional**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
> Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
> Bit 7: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled
> Bit 6: **CRx6**
  - 0: CRx6 disabled
  - 1: CRx6 enabled
> Bit 5: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled
> Bit 4: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled
> Bit 3: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
> Bit 2: **Vbias enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
> Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.15: ATI Base and Target

Register:	0xB001, 0xB101, 0xB201, 0xB301, 0xB401, 0xB501, 0xB601, 0xB701, 0xB801, 0xB901, 0xBA01, 0xBB01, 0xBC01, 0xBD01, 0xBE01, 0xBF01, 0xC001, 0xC101,0xC201, 0xC301														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

> Bit 8-15: **ATI Target**
  - 8-bit value * 8
> Bit 3-7: **ATI Base**
  - 5-bit value * 16

- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

Table A.16: Fine and Coarse Multipliers

Register:	0xB002, 0xB102, 0xB202, 0xB302, 0xB402, 0xB502, 0xB602, 0xB702, 0xB802, 0xB902, 0xBA02, 0xBB02, 0xBC02, 0xBD02, 0xBE02, 0xBF02, 0xC002, 0xC102,0xC202, 0xC302														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.17: ATI Compensation

Register:	0xB003, 0xB103, 0xB203, 0xB303, 0xB403, 0xB503, 0xB603, 0xB703, 0xB803, 0xB903, 0xBA03, 0xBB03, 0xBC03, 0xBD03, 0xBE03, 0xBF03, 0xC003, 0xC103,0xC203, 0xC303														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.18: Filter Betas

Register:	0xC400														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Counts Low Power Beta				Counts Normal Power Beta				LTA Low Power Beta				LTA Normal Power Beta			

- Bit 12-15: **LTA Low Power Beta Filter Value**
  - 4-bit value
- Bit 8-11: **LTA Normal Power Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Counts Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Counts Normal Power Beta Filter Value**
  - 4-bit value

Table A.19: Fast Filter Betas

Register:	0xC401														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- Bit 4-7: **LTA Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
  - 4-bit value

Table A.20: Control Settings

Register:	0xD0														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Interface type		Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 6-7: **Interface Selection**

- 00: I²C streaming
- 01: I²C event mode
- 10: I²C Stream in touch

> Bit 4-5: **Power Mode Selection**
- 00: Normal power
- 01: Low power
- 10: Ulta-low Power
- 11: Automatic power mode switching

> Bit 3: **Execute Reseed Command**
- 0: Do not reseed
- 1: Reseed

> Bit 2: **Execute ATI Command**
- 0: Do not ATI
- 1: ATI

> Bit 1: **Soft Reset**
- 0: Do not reset device
- 1: Reset device

> Bit 0: **Acknowledge Reset Command**
- 0: Do not acknowledge reset
- 1: Acknowledge reset

Contact Information

	USA	Asia	South Africa
Physical Address	11940 Jollyville Rd Suite 120-S Austin TX–78759 USA	Room501A, Block A T-Share International Centre Taoyuan Road Nanshan District Shenzen Guangdong Province PRC	1 Bergsig Avenue Paarl 7646 South Africa South Africa
Postal Address	11940 Jollyville Rd Suite 120-S Austin TX–78759 USA	Room501A, Block A T-Share International Centre Taoyuan Road Nanshan District Shenzen Guangdong Province PRC	PO Box 3534 Paarl 7620 South Africa South Africa
Tel	+1 512 538 1995	+86 755 8303 5294 ext 808	+27 21 863 0033
Email	info@azoteq.com	info@azoteq.com	info@azoteq.com

Visit www.azoteq.com
for a list of distributors and worldwide representation.